swissbit®

Product Data Sheet

Industrial SDHC Memory Card

S-220 Series

SPI, SDHC compliant, class 6 & 10 compliant

BU: Flash Products
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made in germany

S-220 Series
SDHC Memory Card

1 Feature summary

- Custom-designed, highly-integrated memory controller
  - Fully compliant with SD Memory Card specification 2.0
  - Four integrated 4KByte Sector Buffers for fast data transfer
  - SPI Mode support
- Standard SD Memory Card form factor
  - 32.0mm x 24.0mm x 2.1mm
  - Write Protect slider
- 2.7...3.6V normal operating voltage
- 2.0...3.6V basic communication (CMD0, 15, 55 ACMD41) voltage
- Low-power CMOS technology
- Patented power-off reliability
  - No data loss of older sectors
  - Max. 32 sectors data loss (old data kept) if power off during writing before card status is ready
- Wear Leveling: equal wear leveling of static and dynamic data
  The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed.
- Write Endurance: Due to intelligent wear leveling an even use of the entire flash is guaranteed, regardless how much "static" (OS) data is stored.
  Example: If the average file size is 10MByte and the total capacity is 8GByte, 80Mio write cycles can be performed.
- High reliability
  - Best available SLC NAND Flash technology
  - Designed for embedded market
  - MTBF > 4,000,000 hours
  - Number of card insertions/removals: >10,000
  - Extended Temperature range -25° up to 85°C
  - Optional industrial Temperature range available -40° up to 85°C
- Hot swappable
- High performance
  - SD burst up to 25MB/s
  - SD Low speed 0...25MHz clock rate
  - SD High speed 25...50MHz clock rate
  - 2 channel flash
  - Flash burst up to 40MB/s per channel
  - Swissbit S-220 SDHC memory cards are specified as SD 2.0 compliant.
  - Compliant with the highest speed "class 6" according SD2.0 2.0 standard & **speed "class 10"** as defined in SD Specification 3.0.
- Available densities
  - 4GByte and 8GBytes (lower densities are in the SDHC S-200 Series)
- Controlled BOM
- Life Time Monitoring SD/SPI with standard or vendor commands

2 Order Information

2.1 Extended and Industrial Temperature range

Table 1: Product List for standard products

Capacity	Part Number
4GB	SFSD4096LgBN2TO-t-Q2-1x1-STD
8GB	SFSD8192LgBN2TO-t-N2-1x1-STD

g defines the latest product generation,
x defines the latest FW
t defines the temperature range (E=-25°C to +85°C, I=-40°C to +85°C)

2.2 Current product list

Table 2: General Product List

Capacity	Part Number
4GB	SFSD4096L1BN2TO-E-Q2-151-STD
8GB	SFSD8192L1BN2TO-E-N2-151-STD
4GB	SFSD4096L1BN2TO-I-Q2-151-STD
8GB	SFSD8192L1BN2TO-I-N2-151-STD

2.3 Offered options for customer projects

- Customer specified strings and IDs (MID, OID, PNM, PRV)
- Customer specified capacities
- Preload service
- Customized labels
- Customized colors and packages
- permanent write protected with preloaded software
- Option for special FW like:
  - write protection with password (on request)
- SMART-like read out current bad blocks and wear level distribution for life time estimation

Contents

3 Product Specification

The SD Memory Card is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.
The Card operates in two basic modes:

- **SD card mode**
- **SPI mode**

The SD Memory Card also supports SD **High Speed mode** with up to 50MHz clock frequency.
The cards are compliant with

- SD Memory Card Specification Part 1, Physical layer Specification V2.00
- SD Memory Card Specification Part 2, File System Specification V2.00

The Card has an internal **intelligent controller** which manages interface protocols, data storage and retrieval as well as hardware RS-code **Error Correction Code (ECC)**, **defect handling, diagnostics and clock control**.
The **wear leveling** mechanism assures an equal usage of the Flash memory cells to extend the life time.
The hardware RS-code ECC allows to detect and correct **4 symbols per 528 Bytes**.

The Card has a **voltage detector** and a powerful **power-loss management feature** to prevent data corruption after power-down.
The power consumption is very low.
The data retention is 10 years.
The cards are offered in 2 temperature ranges

- Extended -25°C...85°C
- Industrial -40...85°C on request

The cards are RoHS compliant and lead-free.

3.1 System Performance

- Swissbit S-220 SDHC memory cards are specified as SD 2.0 compliant.
- Compliant with the highest speed class 6 defined in SD 2.0 standard & speed class 10 as defined in SD Specification 3.0

Table 3: Performance

System Performance		Typ.	max	Unit
Burst Data transfer Rate (max clock 50MHz)			25 (166X)(1)	MB/s
Sustained Sequential Read	4GB	19 (125X) (1)(2)	21 (140X)(1)	
	8GB	19 (125X) (1)(2)	21 (140X) (1)	
Sustained Sequential Write	4GB	17 (110X) (1)(2)	18 (120X) (1)	
	8GB	17 (110X) (1)(2)	18(120X) (1)	

1) ...X are speed grade markings where 1X = 150 kBytes/s. All values refer to Toshiba Flash chips 32Gb or larger SD Memory Card in SD mode 50MHz, cycle time 20ns, write/read file sequential.
2) Sustained Speed measured with Sandisk Mobile mate USB-SD Memory Card reader. It depends on burst speed, flash type and number, and file size

3.2 Environmental Specifications

3.2.1 Recommended Operating Conditions

Table 4: SD Memory Card Recommended Operating Conditions

Parameter	min	typ	max	Unit
Commercial Operating Temperature	0	25	70	°C
Industrial Operating Temperature	-40	25	85	°C
Power Supply VCC (3.3V)	2.7	3.3	3.6	V

Table 5: Current consumption

Current Consumption (type)	typ	max	Unit
Write	80	90	mA
Read	45	60	
Sleep Mode	0.3	0.4	

3.2.2 Recommended Conditions

Table 6: SD Memory Card Recommended Storage Conditions

Parameter	min	typ	max	Unit
Extended Storage Temperature	-40	25	100	°C
Industrial storage Temperature	-40	25	100	°C

3.2.3 Humidity & ESD

Table 7: Humidity & ESD

Parameter	Operating	Non Operating
Humidity (non-condensing)	max 95%	
ESD according to IEC61000-4-2 Human body model ±4 kV 100 pf/1.5 k0hm Machine model ±0.25 kV 200 pf/0 0hm	**Non Contact Pads area:** ±8 kV (coupling plane discharge) ±15 kV (air discharge) Human body model according to IEC61000-4-2	**Contact Pads:** ±4 kV, Human body model according to IEC61000-4-2

3.2.4 Durability

Table 8: Durability

Parameter	Operating	Non Operating
Salt water spray	3% NaCl/35°C; 24h acc. MIL STD Method 1009	
Solar Exposure	1000W/m2 @ 400°C	
Impermeability	IP67	
UV Light Exposure	UV: 254nm, 15Ws/cm2	
Insertions	>10,000	
Drop test	1.5m free fall	
Bending	10N	
Torque	0.15Nm or ±2.5deg	
Bump	25g; 6ms; ±3 x 4000 shocks	
Shock	1000 g max.	
Vibration (peak -to-peak)	15G max.	
Minimum moving force of WP slider	0.4N	

3.3 Physical Dimensions

Table 9: Physical Dimensions

Physical Dimensions	Value	Unit
Length	32.00±0.10	mm
Width	24.00±0.10	
Thickness	2.10±0.15	
Weight (typ.)	2	g

3.4 Reliability

Table 10: Reliability

Parameter	Value
Data Retention	10 years (JEDEC47G)

4 Density specification

Table 11: SD Memory Card density specification

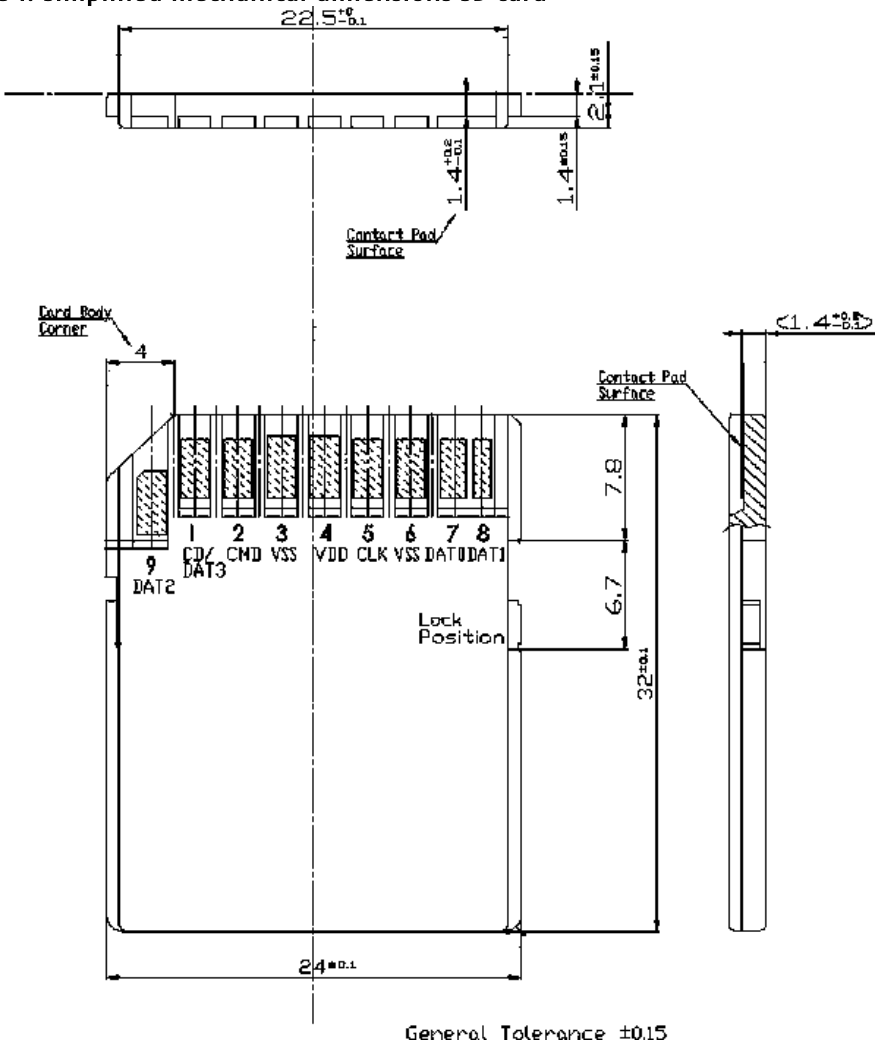
Density	Sectors_card	Total addressable density (Byte)
4GB	8,087,552	4,140,826,624
8GB	16,226,304	8,307,867,648

5 Card physical

5.1 Physical description

The SD Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s).
The dimensions and tolerances are according to the SD specification.

Figure 1: Simplified mechanical dimensions SD card



6 Electrical interface

6.1 Electrical description

Figure 2: SD Memory Card Shape and Interface (Top View)

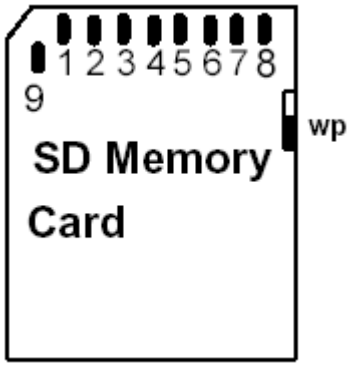


Table 12: SD Memory Card Pad Assignment

Pin #	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type[1]	Description
1	CD/DAT3[2]	I/O/PP[3]	Card Detect/ Data Line [Bit 3]	CS	I[3]	Chip Select (neg true)
2	CMD	PP	Command/Response	DI	I	Data In
3	VSS1	S	Supply voltage ground	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS2	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1[4]	I/O/PP	Data Line [Bit 1]	RSV		
9	DAT2[5]	I/O/PP	Data Line [Bit 2]	RSV		

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers
2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
3) At power up this line has a 50k0hm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command
4) DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).
5) DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

6.2 DC characteristics

Measurements are at Recommended Operating Conditions unless otherwise specified.

Table 13: DC Characteristics

Symbol	Parameter	min	typ	max	unit	notes
I_{DD}	Operating Current Read		50	60	mA	@ 25°C
	Operating Current Write		60	70	mA	@ 25°C
	Pre-initialization Standby Current		150	200	µA	@ 25°C
	Post-initialization Standby Current		130	150	µA	@ 25°C
			400	600	µA	@ 85°C
I_{LI}	Input Leakage Current	-10		10	µA	without pull up R
I_{LO}	Output Leakage Current	-10		10	µA	

Table 14: SD Memory Card Recommended Operating Conditions

Symbol	Parameter		min	typ	max	unit
V_{DD}	Supply Voltage	Normal Operating Status	2.7	3.3	3.6	V
		Basic Communication (CMD0, CMD15, CMD55, ACMD41)	2.0	3.3	3.6	V
-	Power Up Time (from 0V to VDD min)				250	ms

6.3 Signal Loading

according to SD specification

6.4 AC characteristics

6.4.1 Default Speed mode (0 – 25MHz)

according to SD specification

6.4.2 High Speed mode (0 – 50MHz)

according to SD specification

7 Host access Specification

The following chapters summarize how the host accesses the card:

- Chapter 7.1 summarizes the SD and SPI buses.
- Chapter 5summarizes the registers.

7.1 SD and SPI Bus Modes

The card supports SD and the SPI Bus modes. Application can chose either one of the modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. The SD mode uses a 4-bit high performance data transfer, and the SPI mode provides compatible interface to MMC host systems with little redesign, but with a lower performance.

7.1.1 SD Bus Mode Protocol

The SD Bus mode has a single master (host) and multiple slaves (cards) synchronous topology. Clock, power, and ground signals are common to all cards. After power up, the SD Bus mode uses DAT0 only; after initialization, the host can change the cards' bus width from 1 bit (DAT0) to 4 bits (DAT0-DAT3). In high speed mode, only one card can be connected to the bus.
Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

- Command: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command).
  A command is transferred serially on the CMD line.

- Response: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

7.1.2 SPI Bus Mode Protocol

The Serial Parallel Interface (SPI) Bus is a general purpose synchronous serial interface. The SPI mode consists of a secondary communication protocol. The interface is selected during the first reset command after power up (CMD0) and it cannot be changed once the card is powered on.
While the SD channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal.
The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal.
The CS signal must be continuously active for the duration of the SPI transaction (command, response and data).
The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.
The bidirectional CMD and DAT lines are replaced by unidirectional *dataIn* and *dataOut* signals.

The SPI bus signals are listed Table 15 and the SPI bus topology is illustrated in **Fehler! Verweisquelle konnte nicht gefunden werden.**.

Table 15: SPI Bus Signals

Signal	Description
/CS	Host to card chip select
CLK	Host to card clock signal
Data In	Host to card data signal
Data Out	Card to host data signal
Vdd, Vss	Power and ground

7.1.3 Mode Selection

The SD Memory Card wakes up in the SD mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0) and the card is in *idle_state*. If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode.
If SPI mode is required the card will switch to SPI and respond with the SPI mode R1 response.
The only way to return to the SD mode is by entering the power cycle. In SPI mode the SD Memory Card protocol state machine is not observed. All the SD Memory Card commands supported in SPI mode are always available.
During the initialization sequence, if the host gets Illegal Command indication for ACMD41 sent to the card, it may assume that the card is Multimedia Card. In that case it should re-start the card as Multimedia Card using CMD0 and CMD1.

7.2 Card Registers

The SD Memory Card has five registers. Refer to Table 16 to Table 21 for detail.

Table 16: SD Memory Card registers

Register Name	Bit Width	Description	Function
CID	128	Card Identification information	This register contains the card identification information used during the Card Identification phase.
OCR	32	Operation Conditions Registers	This register describes the operating voltage range and contains the status bit in the power supply.
CSD	128	Card specific information	This register provides information on how to access the card content. Some fields of this register are writeable by PROGRAM_CSD (CMD27).
SCR	64	SD Memory Card's Special features	This register provides information on special features.
RCA	16	Relative Card Address	This register carries the card address is SD Memory Card mode.

Table 17: CID register

Register Name	CID slice	Bit Width	Description	typ. value
MID	[127:120]	8	Manufacture ID	0x5d
OID	[119:104]	16	OEM/Application ID	0x5342
PNM	[103:64]	40	Product Name	"L3BN2"
PRV	[63:56]	8	Product Version	0x05 can change
PSN	[55:24]	32	Product Serial Number	xxxxxxxx
–	[23:20]	4	Reserved	0x0
MDT	[19:8]	12	Manufacture Date	0xyym
CRC	[7:1]	7	Check sum of CID contents	chksm
–	[0:0]	1	Not used; always=1	1

Table 18: OCR register

OCR bit position	VDD voltage window	typ. value	OCR bit position	VDD voltage window	typ. value
0-3	Reserved	0	15	2.7-2.8	1
4	1.6-1.7	0	16	2.8-2.9	1
5	1.7-1.8	0	17	2.9-3.0	1
6	1.8-1.9	0	18	3.0-3.1	1
7	1.9-2.0	0	19	3.1-3.2	1
8	2.0-2.1	0	20	3.2-3.3	1
9	2.1-2.2	0	21	3.3-3.4	1
10	2.2-2.3	0	22	3.4-3.5	1
11	2.3-2.4	0	23	3.5-3.6	1
12	2.4-2.5	0	24-30	Reserved	
13	2.5-2.6	0	30	Card Capacity Status (CCS)	*(1)
14	2.6-2.7	0	31	0=busy; 1=ready	*(2)

1) This bit is valid only when the card power up status bit is set.
2) This bit is set to LOW if the card has not finished the power up routine.

Table 19: CSD register

Register Name	CSD slice	Bit Width	Description	typ. Value
		>2Gb		>2Gb
CSD_STRUCTURE	[127:126]	2	CSD structure	01
–	[125:120]	6	Reserved	000000
TAAC	[119:112]	8	Data read access time 1	00001110
NSAC	[111:104]	8	Data read access time 2 (CLK cycle)	00000000
TRAN_SPEED	[103:96]	8	Data transfer rate	00110010
CCC	[95:84]	12	Card command classes	010110110101
READ_BL_LEN	[83:80]	4	Read data block length	1001
READ_BL_PARTIAL	[79:79]	1	Partial blocks for read allowed	0
WRITE_BLK_MISALIGN	[78:78]	1	Write block misalignment	0
READ_BLK_MISALIGN	[77:77]	1	Read block misalignment	0
DSR_IMP	[76:76]	1	DSR implemented	0
–	[75:70]	6	Reserved	000000
C_SIZE	[69:48]	22	Device size	xxx(1)
–	[47:47]	1	Reserved	0
ERASE_BLK_EN	[46:46]	1	Erase single block enable	1
SECTOR_SIZE	[45:39]	7	Erase sector size	1111111
WP_GRP_SIZE	[38:32]	7	Write protect group size	0000000
WP_GRP_ENABLE	[31:31]	1	Write protect group enable	0
–	[30:29]	2	Reserved	00
R2W_FACTOR	[28:26]	3	Write speed factor	010
WRITE_BL_LEN	[25:22]	4	Write data block length	1001
WRITE_BL_PARTIAL	[21:21]	1	Partial blocks for write allowed	0
–	[20:16]	5	Reserved	00000
FILE_FORMAT_GRP	[15:15]	1	File format group	0 W(*)
COPY	[14:14]	1	Copy flag	0 W(*)
PERM_WRITE_PROTECT	[13:13]	1	Permanent write protection	0 W(*)
TMP_WRITE_PROTECT	[12:12]	1	Temporary write protection	0 W
FILE_FORMAT	[11:10]	2	File format	00 W(*)
–	[9:8]	2	Reserved	00 W
CRC	[7:1]	7	Checksum of CSD contents	xxxxxxx W
–	[0:0]	1	Always=1	1

1) Drive Size and block sizes vary with card capacity
memory capacity = (C_SIZE+1) * 512kByte

W value can be changed with CMD27 (PROGRAM_CSD)
W(*) value can be changed ONCE with CMD27 (PROGRAM_CSD)

Table 20: SCR register

Field	SCR Slice	Bit Width	typ Value
SCR_STRUCTURE	[63:60]	4	0000
SD_SPEC	[59:56]	4	0010
DATA_STAT_AFTER_ERASE	[55:55]	1	1
SD_SECURITY	[54:52]	3	011
SD_BUS_WIDTHS	[51:48]	4	0101
Reserved	[47:32]	16	0[1]
Reserved	[31:0]	32	0

1) Bit 47=0 → card is SD2.0 compliant
(therefore marked as speed class 6, but fulfill performance of speed class 10)

Table 21: RCA register

Field	Bit Width	typ Value
RCA	16	0x0000[1]

1) After Initialization the card can change the RCA register.

8 Card Lifetime Information Data

Swissbit S-200/S-220 cards provide various lifetime monitoring information in the "reserved for manufacturer" field of the SD Status register. This data can be read out using ACMD13 (SD_STATUS) on host systems with a native SD-Interface (e.g. embedded systems, SD or SPI interface or PCI/SD-reader).
We recommend assessing the expected/guaranteed life time of Flash based devices to make sure the product life time fulfills your expectations. The real application workload should be tested in a test installation or simulation for best accuracy.
In general, calculations based on application behavior statistics are not possible as the influence of the operating systems (with the caches) and the file system have a big influence on the data actually written on the device.
This product does report the real erase cycles that the NAND Flash blocks have seen. Based on the average erase count and it's ascend in the target system, it is possible to quite simply calculate the expected life time of the product.
Bad and spare block counts can't be used for linear life time calculations. In the beginning of the device life time, only very few blocks will be needed to be replaced. Generally if a device reaches the end of the lifetime, more bad blocks will occur.
The SD Status is defined by the SD Standard and contains several status bits as well as a field for manufacturer specific data. The overall size of the SD Status is one data block of 512 bits divided into 312 reserved for manufacturer bits used for the Swissbit lifetime information and 200 bits for other purposes, defined by the SDA.
The content of the SD Status register is transmitted to the Host over the DAT bus along with a 16-bit CRC. The SD Status is sent to the host over the DAT bus as a response to ACMD13 (CMD55 followed with CMD13). ACMD13 can be sent to a card only in "tran_state" (card is selected).

Please note that it is not possible so set up the necessary command (ACMD13) through a common USB/SD-card reader/bridge. In contrast to that, a lot of embedded systems and PCIe card readers support the command.

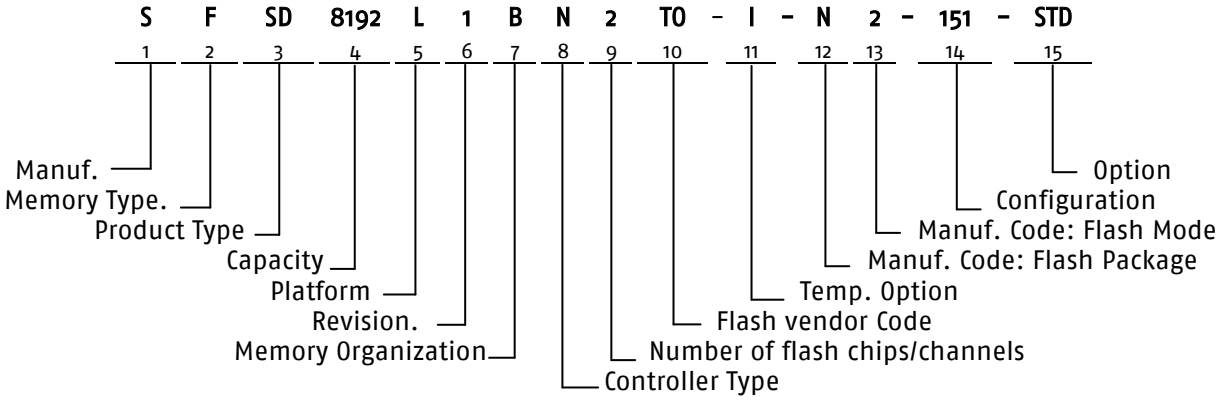
Swissbit provides a demo code written in C for Linux systems on demand.

Table 22: SD Status and Lifetime Information sector decoding

Bits	Description (All values MSb first)
[511:312]	SD Status field as defined in the Physical Layer Specification Version 2.00 (Not relevant for Card Lifetime Info)
[311:304]	Data structure version identifier ("0" for S-200/S-220 cards)
[303:288]	Number of initial defect blocks
[287:272]	Number of initial spare blocks, 1st flash CE (across channels) big Endian
[271:256]	Number of initial spare blocks, 2nd flash CE (across channels) big Endian
[255:248]	Percentage of remaining spare blocks, first flash CE (across channels)
[247:240]	Percentage of remaining spare blocks, second flash CE (across channels)
[239:224]	(Reserved)
[223:192]	(Reserved)
[191:176]	Lowest wear level class (WL)
[175:160]	Highest wear level class (WH)
[159:144]	Wear level threshold (T)
[143:96]	Total number of block erases
[95:80]	Number of flash blocks
[79:64]	Maximum flash block erase count target, in wear level class units
[63:32]	Power on count
[31:24]	(Reserved)
[23:16]	(Reserved)
[15:8]	(Reserved)
[7:0]	(Reserved)

The lowest wear level class (WL) and highest wear level class (WH) fields give the range of wear level classes currently in use. The wear level threshold (T) gives the size of a wear level class, minus 1, in units of flash memory block erases. Thus, the number of block erases that the flash blocks have seen is between WL*(T+1) and WH*(T+1)-1.

9 Part Number Decoder



1. Manufacturer

Swissbit code	S

2. Memory Type

Flash	F

3. Product Type

SD Memory Card	SD

4. Capacity

4 GB	4096
8 GB	8192
16 GByte	16GB
32 GByte	32GB

5. Platform

SD Memory Card	L

6. Revision

7. Memory Organization

x8	B
x16	C

8. Controller type

SD Memory Card controller	S-2xo series	N

9. Channels

1 Flash Channel	1
2 Flash Channel	2

10. Flash Code

Samsung	SA
Toshiba	TO

11. Temp. Option

Industrial Temp. Range -40°C – 85°C	I
Extended Temp. Range -25°C – 85°C	E

12. DIE Classification

SLC MONO (single die package)	M
SLC DDP (dual die package)	D
SLC QDP (quad die package)	Q
SLC ODP (octal die package)	N

13.

14. PIN Mode

Normal nCE & R/nB	0
Dual nCE & Dual R/nB	1
Quad nCE & Quad R/nB	2

15. Configuration XYZ

X→ Configuration

Configuration	X
default	1

Y → FW Revision

FW Revision	Y
Revision 1	1
Revision 2	2
Revision 3	3
Revision 4	4
Revision 5	5
Revision 7	7

Z → optional

Optional	Z
optional	1

16. Option

Swissbit / Standard	STD

10 Swissbit Label specification

10.1 Front side label

4GB SDHC Memory Card – class 6
(class 10 compliant)

8GB SDHC Memory Card – class 6
(class 10 compliant)

Cards are labeled with speed class 6 because they are compliant with SD specification 2.0, but speed class is only specified in SD specification 3.0.
Nevertheless, Swissbit S-220 cards fulfill all performance requirements for speed class 10.

10.2 Back side lasering

SWISSBIT
SFSDXXXXLXBN2
T0-X-XX-1X1-XXX
5013-6131210X
Made in Germany
CE WEEE

Part-number
calendar week and year – Lot code

Example of the back side laser marking

11 Revision History

Table 23: Document Revision History

Date	Revision	Description	Revision Details
April 13, 2010	1.00	S-220 cards with Toshiba flash	
September 28,2010	1.01	SDHC 4GB PN with Q2 instead of Q1, higher storage temperature for extended cards	
January 03, 2012	1.02	Performance value updated, label and lasering update	
April 27, 2012	1.10	SDA Correction, CI update	
December 11, 2012	1.20	New CE Declaration, new picture back side lasering	
March 25, 2013	1.30	Performance compatible to speed class 10, CID, CSD, SCR bit slices added	
September 20, 2013	1.31	High-Speed SD bus timing diagram corrected	
October 11, 2013	1.32	Low-Speed SD bus timing diagram corrected	
February 17, 2014	1.33	DC and AC characteristics updated to SDA 3.0 specification, CE Declaration removed	
February 12, 2015	1.34	Added chapter 8 "Card Lifetime Information Data"	
July 04, 2016	1.40	Updated Chapter 5, 6, 7, back side lasermarking, removed RoHS/WEEE decl. and added feature icons	Doc. req. no. 1157
Otober 24, 2016	1.41	Current values updated	Doc. req. no. 1352