swissbit®

EM-10 e•MMC Routing Guideline

Application Note

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1 Overview

The Swissbit® EM-10 is an e·MMC™ (eMMC) flash-based device designed to operate reliably under embedded and industrial conditions. These devices follow the JEDEC eMMC 4.41 Standard (JESD84-A441) in a ball grid array (BGA) 153-ball package. Because the signals and footprint follow the industry-standard design rules, the printed circuit board (PCB) routing can be manufactured with state-of-the-art PCB processes. This document provides guidelines for signal and power layout as well as suggestions for the BGA layout.

This document is valid for the EM-10 part numbers listed in the following table.

Table 1: EM-10 Part Numbers

Density	Part Number	Temp. Range	Flash Technology
4 GB	SFEM4096B1EM1T0-A-GE-111-STD	-40°C to 105°C	MLC NAND Flash
8 GB	SFEM008GB1EM1T0-A-LF-111-STD		
16 GB	SFEM016GB1EM1T0-A-HG-111-STD		

2 General Guidelines

This section provides a general layout routing guide for PCBs using eMMC. For accurate signal and power integrity analysis, a PCB simulation is recommended. When operating with 52 MHz, the PCB design must follow common high-speed rules. Additional guidelines include the following:

- The CLK net is the most critical signal.
- DS (data strobe) is not used by EM-10. If compatibility to higher eMMC standards (eMMC 5.0) is desired then DS should be routed similar to CLK
- Signals DAT0-DAT7, CLK, and CMD must have the same trace length for better timing.
- For reduced interference:
    - Use wider spacing between signals to avoid crosstalk.
    - Avoid duplication between the upper and lower signals in non-reference plane structures.
    - Use the shortest signal lengths possible to reduce crosstalk length.
    - Avoid reflection interference by using the shortest branch lengths possible.
- Wide trace widths and short signal lengths will reduce power bus resistance and inductance and minimize voltage drops.
- Decoupling caps should be placed as close to the controller pad as possible to minimize voltage noise.

3 Signal Description

The following table lists the pin numbers, the type, and the function associated with the signals of the EM-10.

Table 2: EM-10 Signals

Pin Number(s)	Symbol	Type	Ball Function
M6	CLK	I	**Clock:** Each cycle directs a one-bit transfer on the CMD and DAT lines.
M5	CMD	I/O	**Command:** A bidirectional channel used for device initialization and command transfer. This signal has two operating modes: 1. Open-drain for initialization. 2. Push-pull for fast command transfers.
A3	DAT0	I/O	**Data 0-7:** Bidirectional channels used for data transfer.
A4	DAT1	I/O	
A5	DAT2	I/O	
B2	DAT3	I/O	
B3	DAT4	I/O	
B4	DAT5	I/O	
B5	DAT6	I/O	
B6	DAT7	I/O	
K5	RST_n	I	**Reset:** Reset signal pin, only works, if functionality is activated in extended CSD
E6, F5, J10, K9	V_{CC}	Supply	**Supply Voltage:** Flash memory and flash memory interface power supply.
C6, M4, N4, P3, P5	V_{CCQ}	Supply	**I/O Voltage:** Memory controller core regulator and MMC interface I/O power supply.
A6, E7, G5, H10, J5, K8	V_{SS}	Supply	**Core Regulator Supply Voltage Ground:** Flash memory interface and flash memory ground connection.
C4, N2, N5, P4, P6	V_{SSQ}	Supply	**I/O Supply Voltage Ground:** Memory controller core and MMC interface ground connection.
C2	V_{DDi}		**Internal Core Logic Voltage:** Connect an external 2.2 µF capacitor to GND.
H5	NC (DS)	0	**Data Strobe:** not connected, only for HS400 mode (not supported)
	NC		**No Connect:** Can be connected to ground or left floating.
A7, E5, K6, K7	RFU		**Reserved for future use:** do not connect
E8, E9, E10, F10, F11, K11, P11	VSF		**Vendor Specific Function:** do not connect

See the following sections for the signal and power layout guidelines.

3.1 eMMC Signal Layout Guidelines

Signal routing should be implemented either in Microstrip line or Stripline as long as the trace impedance is maintained for all signals at 50 ohm ± 10%. See Figure 1 for the line definitions.

The suggested total signal trace lengths is <2000 mil.

The signal trace length skew constraints are as follows:

- **ABS (CLK-DAT0~DAT7):** 250 mil
- **ABS (CLK-CMD):** 250 mil
- **ABS (CLK-RST_N):** 1000 mil

The signal spacing constraints from other signals are:

- **DAT0~DAT7, CMD:** > 2H
- **RST_N:** > 1.5H

For these constraints, *H* is the height of the dielectric between signal and GND (reference layer).

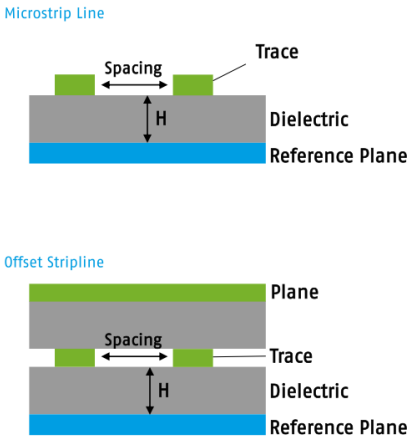

Figure 1: Line Definitions

Recommendations for the signal branch include:

- Keep the signal trace branch lengths below 200 mil.
- Place the CLK test pad (if present) as close as possible to the eMMC package.

If there is enough space, it is recommended to use the GND (ground) shielding to reduce crosstalk effects between the eMMC signals.

3.2 eMMC Pad Layout Guidelines

There are two types of PAD layouts: "Solder mask define" (SMD) and "Non solder mask defined" (NSDM).

The differences are shown in Figure 2.

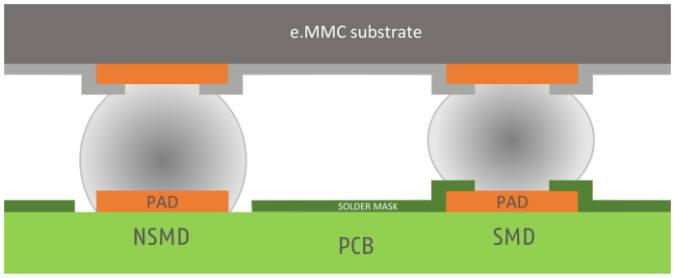

Figure 2: SMD and NSDM pad

For the SMD pad the opening and exposed copper is smaller than for the NSDM. NSDM pads provide better robustness against temperature stress but have a higher risk that the pad lifts off during the solder process or rework.

For 0.5mm ball diameter it is recommended to use the NSMD pad layout.

The suggested pad settings are:

- Pad type: NSMD
- Pad pitch: 500µm (~20mils)
- Pad size: 250µm (~10mils)
- Mask shape: Round
- Mask opening: 50µm around pad (350µm antipad for the 250µm pad)
- Mask width between pads: 150µm
- Trace between pads: allowed with 3.2mil trace maximum
- Trace width: 82µm (~3.2mil)
- Pad to trace clearance: 82µm (~3.2mil)

3.3 eMMC Power Layout Guidelines

For the decoupling capacitor, Swissbit recommends the following:

- **Type:** X7R or X5R
- **Rated Voltage:** 6.3 V
- **Size:** As small as possible to be positioned close to the BGA power balls

The following table lists the recommended minimum decoupling capacitor charges and quantity for different power signals. In addition, the target ball location on the BGA is provided. When placing the decoupling capacitors, they should be located as closely as possible to the target balls. See section 5.1 for the BGA layout recommendation.

Table 3: Decoupling Capacitor Recommendations

Supply	Quantity	Capacity	Target Ball(s)
V_{CCQ}	1	0.1 µF	C6, M4, N4, P3, P5
	1	4.7 µF	
	1	1.0 µF*	
V_{CC}	1	0.22 µF	E6, F5, J10, K9
	1	4.7 µF	
V_{DDi}	1	0.1 µF	C2
	1	2.2 µF	

* This capacitor should be placed as close as possible to C6.

For the power and ground traces:

- Design trace width as wide as possible (~15 mil).
- Implement dedicated power/GND planes, if possible.

4 BGA 153 Ball Reference Design Schematics

The following figure shows the ball reference design for the EM-10 BGA. For information about the specific signals, see table 2.

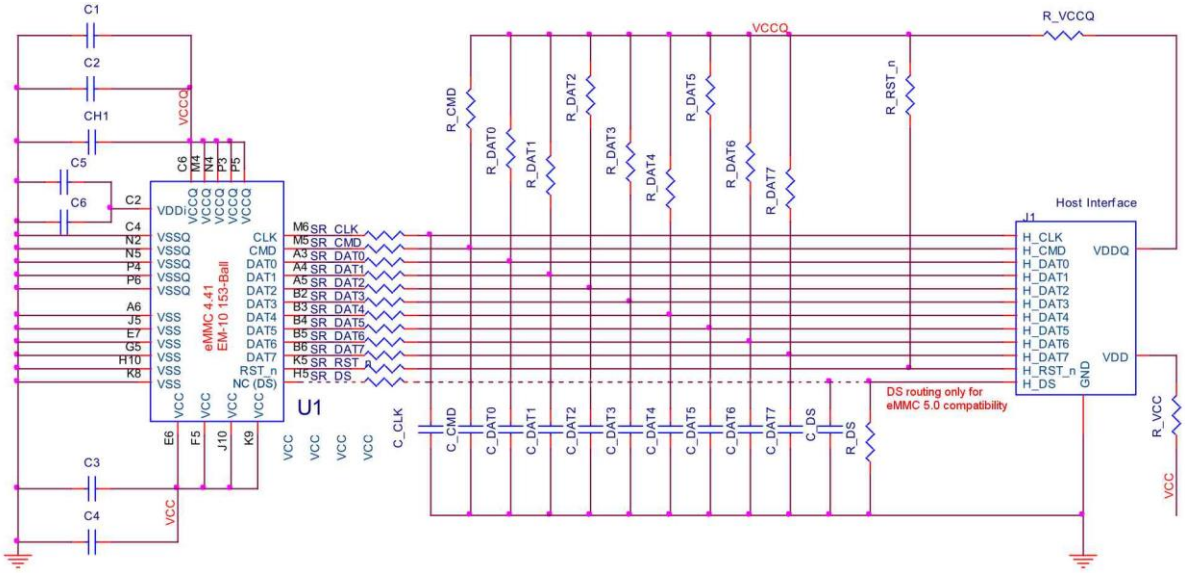

Figure 2: EM-10 Reference Schematics

Table 4: BGA Reference Design Parameters

Parameter	Symbol(s)	Min	Max	Typ	Units	Remark
Pull up resistance for CMD	R_CMD	4.7	50	10	kΩ	Prevents bus floating.
Pull up resistance for DATA0-7	R_DAT	10	50	10	kΩ	Prevents bus floating.
Pull up resistance for RST_n	R_RST_n	4.7	50	10	kΩ	Can be omitted if host does not use H/W reset (EXT_CSD Register [162]=0b).
Pull down resistance for DS	R_DS	10	50	10	kΩ	Not necessary for EM-10
Impedance for CLK / CMD / DATA0~7		45	55	50	Ω	Impedance match.
Serial resistance on CLK line	SR_CLK	0	47	0	Ω	
Serial resistance on CMD, DS, DAT0-7, RST_n	SR_RST_n SR_DS SR_CMD SR_DAT0~7	0	47	0	Ω	SR_DS not necessary for EM-10
Parallel capacitor on CLK, CMD, DS, DAT0-7	C_CLK C_CMD C_DS C_DAT0~7	0	5	0	pF	C_DS not necessary for EM-10
V_{CCQ} capacitor value	C1	2.2	4.7	4.7	µF	Coupling capacitor should be connected as closely as possible to V_{CCQ} and V_{SSQ}.
	C2	0.1	0.22	0.1	µF	
	CH1	1	2.2	1	µF	CH1 should be placed adjacent to the V_{CCQ} and V_{SSQ} balls (C6 and C4, respectively). It should be located as closely as possible to these balls to minimize parasitic capacitance.
V_{CC} capacitor value	C3	2.2	4.7	4.7	µF	Coupling capacitors should be connected as closely as possible to V_{cc} and V_{SS}.
	C4	0.1	0.22	0.22	µF	
V_{DDi} capacitor value	C5	2.2	4.7	2.2	µF	Coupling capacitors should be connected as closely as possible to V_{DDi} and V_{SS}.
	C6	0.1	0.22	0.1	µF	

5 BGA 153 Layout Recommendations

5.1 BGA 153 Ball Layout

The following figure provides the BGA layout recommendation.

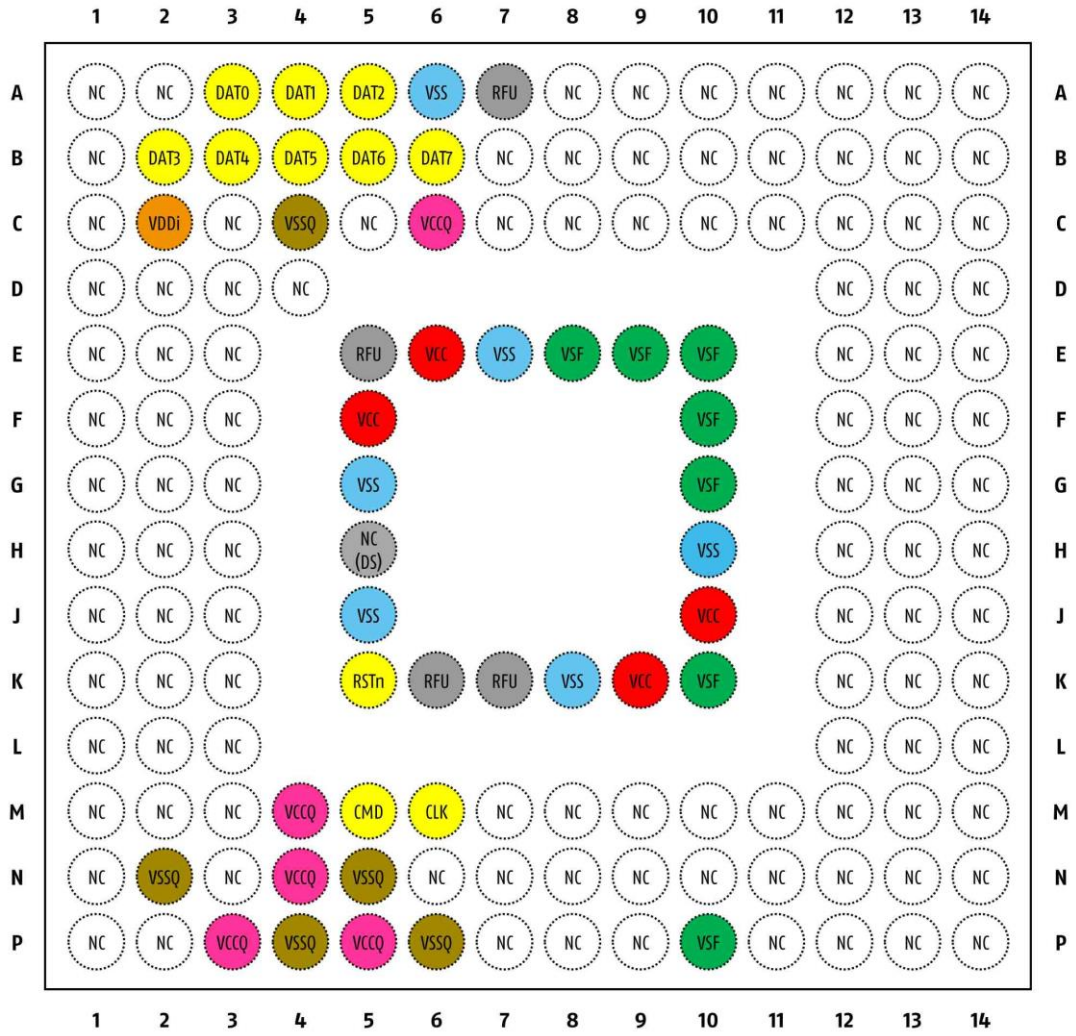

Figure 3: BGA Layout

Note: Do not connect the RFU and VSF balls. These are reserved for future use.
VSF balls could be connected to test pads for debugging, especially:

P10: ROM Boot
F10, G10, K10: Debug interface

NC (DS) pin is not used for EM-10 operation, but required by higher e.MMC standards

Unshielded signal traces and vias of from other devices under the eMMC footprint should be avoided to limit crosstalk and shorts.

5.2 BGA 153 Ball Layout Capacitor Positioning

The recommended capacitor locations are illustrated in the following figure.

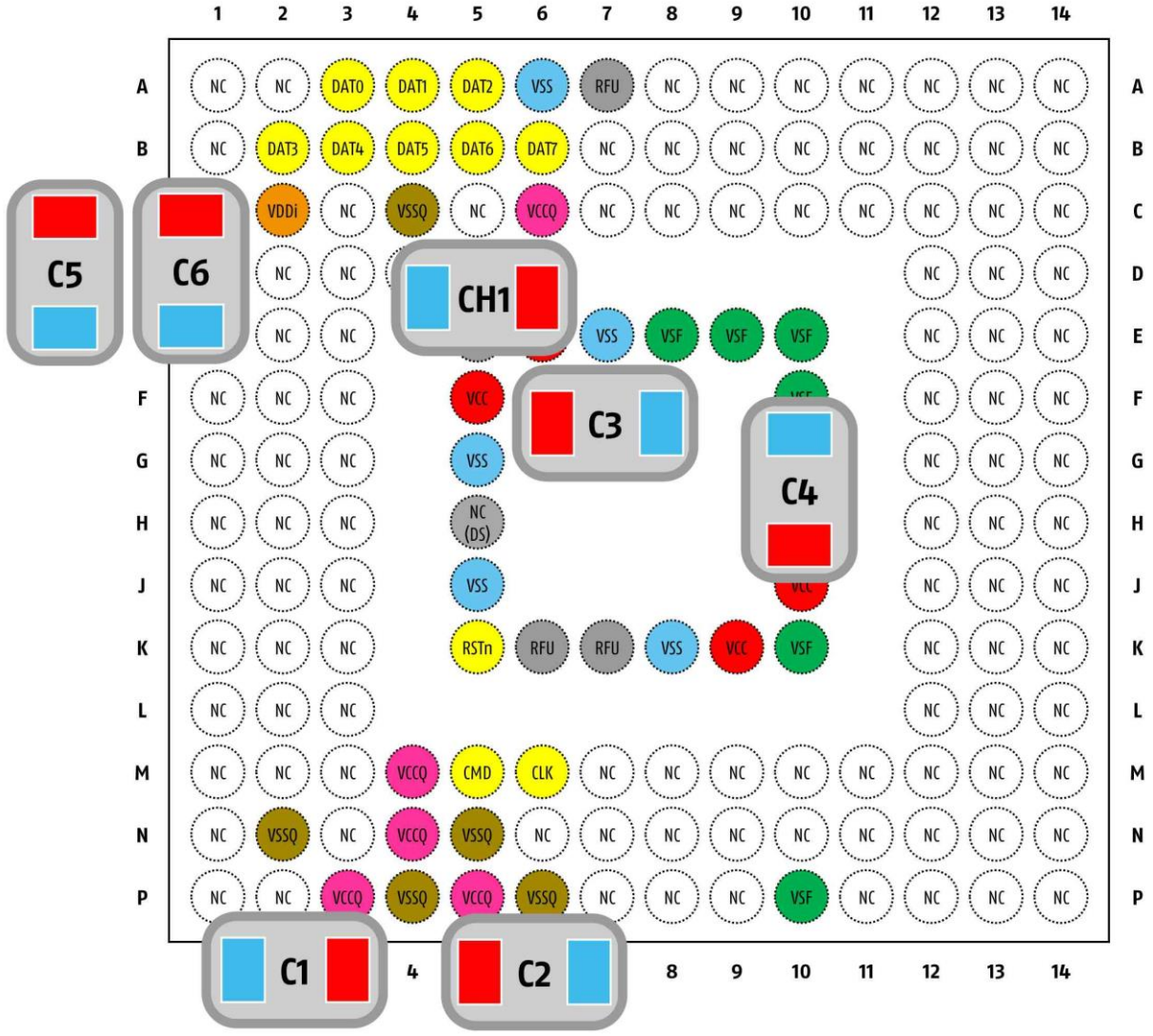

Figure 4: Capacitor Location Recommendations

Minimum requirement for C5 (C_{reg} at V_{DDi} pin): **C5 min = 2.2 µF**

Recommendations: Type: 6.3V, X5R, placement close to e.MMC BGA C2 pin

5.3 BGA 153 Ball Layout High Speed Signal Breakout Example

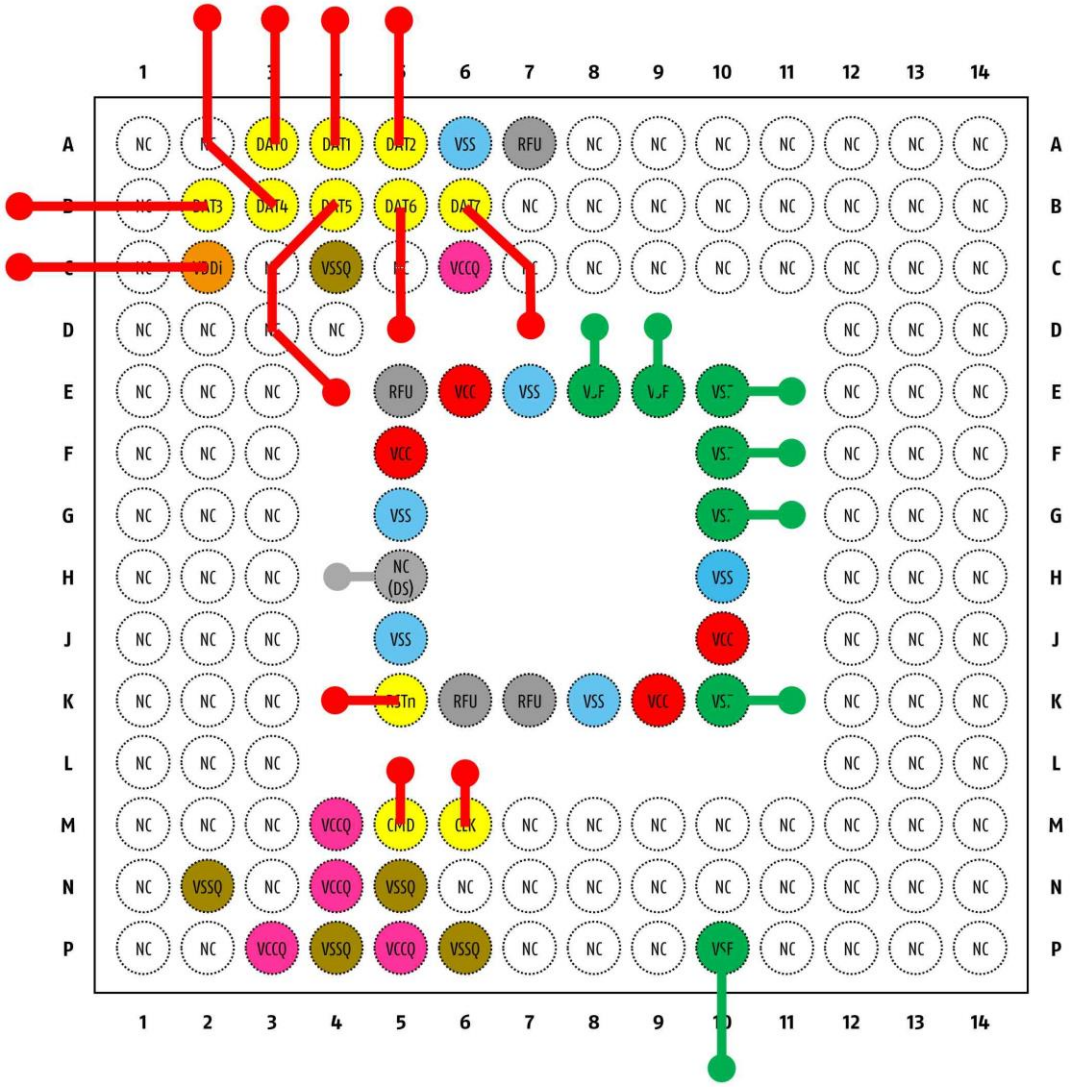

Figure 5: High Speed Example

Routing the high speed signals over a maximum of two no connect (NC) pins is allowed. To compensate for the different capacitive loading of the NC ball signals, use a shorter trace routing length.

DS routing is not necessary for EM-10 but is suggested for compatibility with e.MMC5.x speed

5.4 Supply voltage requirements

To prevent undefined device behavior, the time difference between reaching VCCmin and VCCQmin (or vice versa) should be: **Tdiff < 80ms**

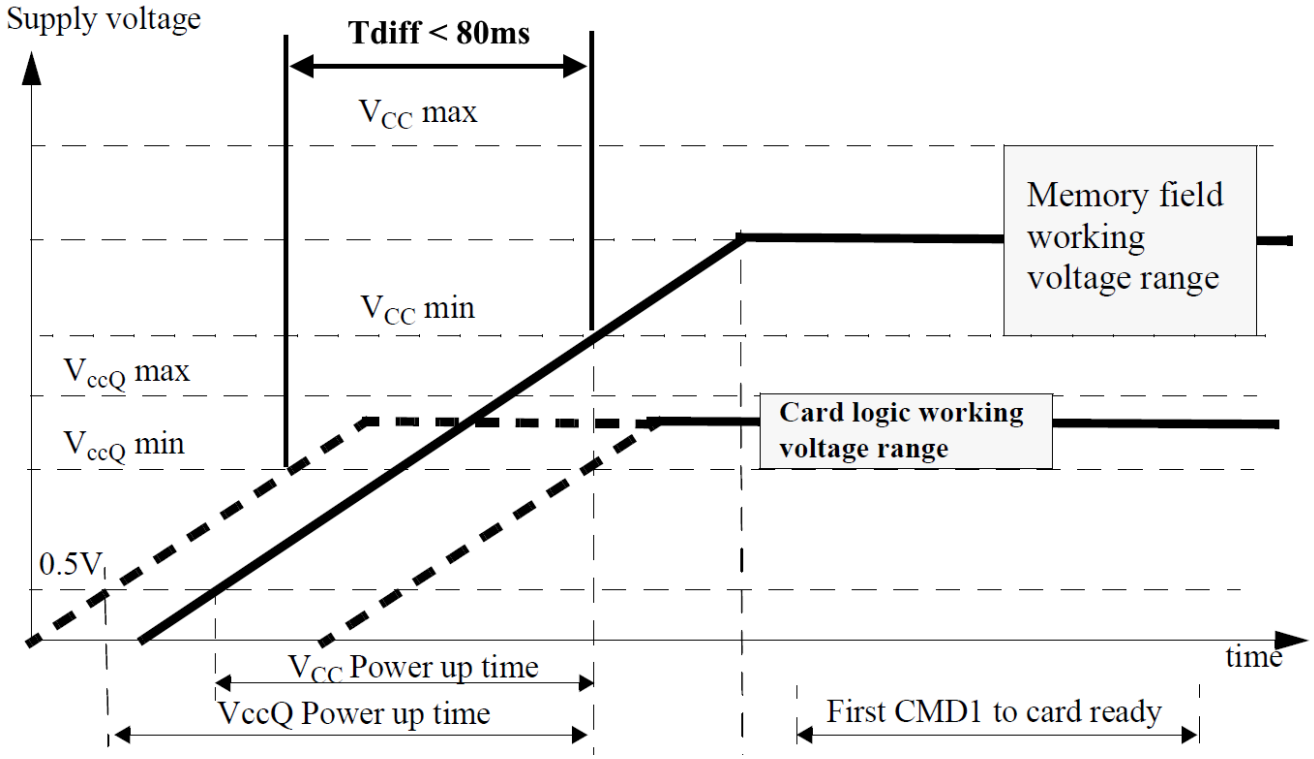

Figure 6: Supply Power up sequence

6 Document History

Table 5: Document Revision History

Date	Revision	Details
03-Oct-2018	1	Initial release

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